REMARKS

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Drawing objections

Applicant notes the objections made to Fig. 1 of the drawings. Instead of amending the drawing, applicants have chosen to amend the specification to conform to the item notations in the figure. No new matter has been added.

Specification objections

Applicants have amended the title as suggested by the Examiner, and have inserted the requested serial number data.

Rejection under 35 USC § 101

Claims 1-8 stand rejected under 35 USC § 101 as not reciting any hardware necessary to render the claims tangible. Applicants have clarified that these claims are directed to a computer program storage device containing a computer-readable program having a memory structure for parallel computing, with the parallel computing memory structure having the first and second hierarchy levels as recited. As described in the specification at page 10, lines 7-19, this invention provides a programming approach that may be stored, for example, in a program or memory storage device. A computer program storage device containing a computer-readable program having a memory structure is tangible. No new matter has been added.

Rejection under 35 USC § 112, second paragraph

Claims 15-18 stand rejected under 35 USC § 112, second paragraph, as being indefinite as to intended metes and bounds. Applicants respectfully traverse this rejection. The program storage device, e.g., a read-only memory (see specification page 21, line 23), contains a program of instructions executable by a machine such as a computer to perform method steps for parallel processing. The method steps for parallel processing use a computer memory having the recited structure of a first level of hierarchy, and so on. The instructions on the program storage device perform the recited method steps of employing the first and second threads, as stated in the claim. These method steps are similar to those recited in claim 11. Accordingly, applicants submit that claims 15-18 meet the requirements of 35 USC § 112, second paragraph.

Rejection under 35 USC § 102

Claims 15-18 stand rejected under 35 USC § 102 as being anticipated by Shimizu U.S. Patent No. 6,038,647. Applicants respectfully traverse this rejection.

Applicants' claims 15-18 describe a program storage device containing instructions to perform the recited method steps for parallel processing using a computer memory having: 1) a first level of hierarchy with, among other things, a plane containing a thread which represents an independent flow of control managed by a program structure, and 2) a second level of hierarchy comprising a space containing two or more of such planes. The method steps include employing first and second threads managed by the program structure to access the specified data in first and second planes, while the threads avoid interaction except when explicitly requested by the program structure.

The present invention provides a programming approach to memory structure. In contrast, Shimizu is directed to a technique applied to hardware, i.e., a cache memory device. While the Shimizu patent discusses parallel process architecture, the "threads" are not comparable to those that applicants claim, and Shimizu's cache memory access method is not what applicants are claiming. While it is difficult to determine precisely what Shimizu means by the term "thread," it appears to involve assignment of data storage priority (Column 8, lines 13-15), and not an independent flow of control managed by a program structure as in applicants' claims. Accordingly, Shimizu does not anticipate (or render obvious) the program storage device recited in applicants' claims 15-18.

Rejection under 35 USC § 103

Claims 1-4, 6-8, 9, 10 and 11

Claims 1-4, 6-8, 9, 10 and 11 stand rejected under 35 USC § 103 as being obvious from Meyer U.S. Patent No. 6,397,299 in view of Cai et al. U.S. Patent Publication No. US2001/0049770A1. Applicants respectfully traverse this rejection.

Claims 1 and 9

Applicants' invention as defined in claims 1-4 and 9 is directed to a computer program storage device containing a computer-readable program having a memory structure for parallel computing (claims 1-4) and a computer program product for parallel computing having computer code defining computer memory structure (claim 9). The parallel computing memory structure has first and second levels of hierarchy. The first level comprises a plane containing a thread which represents an independent flow of control managed by a program structure, heap and stack portions, and local variables and

global data accessible by the program structure. The second level comprises a space containing two or more of the planes, wherein the planes in the space contain the program structure. The space also contains common data accessible by the program structure between each of the planes. As stated in the specification at page 10, lines 17-21, the invention naturally enables the design and implementation of parallel algorithms with minimal and well defined data space interaction, thus providing low cost, high performance parallelism without necessitating the programmer being an expert in the management of parallelism.

Unlike applicants' claimed program-based parallel computing memory structure, the Meyer patent is directed to a method of using non-cacheable memory that is physically distinct from main memory, and appears to use different speed memory for faster access. Meyer never even mentions parallel computing or processing (according to the undersigned's word search on the copy of Meyer on the PTO's web site), and does not teach or suggest applicants' parallel computing memory structure having the claimed first and second levels of hierarchy, and detailed structure therein. Accordingly, Meyer represents non-analogous art, and as such, one of ordinary skill in the art would not combine it with the Cai reference.

Cai is directed to a buffer memory management in a system having multiple execution entities. While Cai makes mention that "the multi-unit data cache system may offer high access bandwidth by increasing parallelism for a multithreading or multitasking processor" (paragraph 0053), the structure of the cache or buffer memories is not comparable to that of applicants' claimed parallel computing memory structure with first

and second levels of hierarchy having the recited features. For example, applicants' first level of hierarchy comprises a plane containing a thread which represents an independent flow of control managed by a program structure, and the second level of hierarchy comprises a space containing two or more of said planes. This structure is simply not disclosed or suggested by Cai's buffer memory structure, or the "program execution entity, such as a ... thread" (paragraph 0005). The Examiner acknowledges as much by admitting that "[t]he references of Meyer modified by Cai fail to teach to form another level of hierarchy." Office action, page 6. The level of detail that the Examiner believes would be "well known in the art" that would modify the non-analogous Meyer reference with Cai to arrive at applicants' invention is simply not obvious to one of ordinary skill in this art. Applicants respectfully request that the Examiner provide some evidence that the missing detail of the hypothetical combination of Meyer and Cai is well known.

Claims 2, 3, 6-8 and 10

Applicants' claims 2, 3, 6-8 and 10 add to the previously described parallel computing memory structure a third level of hierarchy comprising two or more of the spaces containing the same or different program structures having a library of programs, and common data accessible by the program structure between each of the spaces. Again, the admitted lack of evidence in the form of cited prior art to suggest the combination of the claimed three levels of hierarchy in a parallel computing memory structure undercuts any position that claims 6-8 and 10 would be obvious to one of ordinary skill in this art.

Claim 11

Claim 11 is directed to a method of parallel processing which uses the memory structure as described in claim 1, and adds the steps of employing first and second threads managed by the program structure to access the specified data in first and second planes, while the threads avoid interaction except when explicitly requested by the program structure.

The hypothetical combination of the non-analogous Meyer patent with Cai again does not disclose or suggest applicants' claimed memory structure used in its parallel processing method, as discussed above. The EIDs that the Examiner references in the Cai patent are not disclosed as having the same properties as the threads in applicants' claim 11, where the first thread operates in the first plane of the first level hierarchy, and the second thread operates in the space (i.e., two or more planes) of the second level hierarchy, wherein the first and second threads only interact when explicitly requested by the program structure. Cai's EIDs are not disclosed as operating separately on different hierarchy levels, as applicants claim, and therefore the combination of Meyer and Cai cannot render applicants' invention obvious.

Claims 5 and 12-14

Claims 5 and 12-14 stand rejected as being obvious from Meyer and Cai further in view of Arimilli et al. U.S. Patent No. 6,473,833. Applicants respectfully traverse this rejection.

Claim 5

Claim 5 is dependent on claim 2 (which recites the three level hierarchy discussed above) and recites that the structure comprises a library of programs and further add a function table for the space adapted to exchange services with the library in the space.

As stated above, the combination of non-analogous Meyer patent with Cai does not disclose or suggest the invention described in base claim 2, and the Arimilli patent does not make up for the deficiencies of those references. Arimilli is directed to a method of operating a multi-level cache memory of a computer system, and caching with faster access in fast memory as opposed to slow bulk memory. Arimilli uses a defined structure to gain faster access, but does not disclose or suggest the use of first, second and third level hierarchy or the structures of those hierarchies, as in base claim 2. Accordingly, the suggestion by Arimilli of using a "directory of the next lower level of storage" providing a faster access to the directory information (abstract) does not render obvious applicants' library of programs and function table for each space in the second and third hierarchy levels, with the function table adapted to exchange services with the library in each of the spaces.

Claim 12

Claim 12 is dependent on claim 11 and recites that the program structure comprises a library of programs, adds providing a function table for the space adapted to exchange services with the library in the space, and further includes the step of employing the first and second threads to make function calls to the function table to access common data between each of the planes and common data in the space.

Armelli does not disclose or suggest the use of first and second level hierarchy or the structures of those hierarchies, as in base claim 11, or the method of employing first and second threads managed by the program structure to access the specified data in first and second planes, while the threads avoid interaction except when explicitly requested by the program structure. Since the combination of non-analogous Meyer patent with Cai does not disclose or suggest the invention described in base claim 11, the Arimilli patent cannot and does not make up for the deficiencies of those references. Again, Arimilli's use of a "directory of the next lower level of storage" providing a faster access to the directory information (abstract) does not render obvious applicants' library of programs and function table for the space in the second hierarchy level, and the use of the first and second threads to make function calls to the function table to access common data between each of the planes and common data in the space.

Claim 13

Claim 13 adds to base claim 11 the provision of the third level of hierarchy and the step of accessing the common data between each of said spaces by said first and second threads, and is not obvious from a hypothetical combination of Meyer, Cai and Arimilli for the reasons given in connection with claims 5 and 11, discussed above.

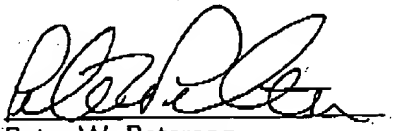
Claim 14

Claim 14 adds to base claim 13 the limitation that the program structure comprises a library of programs, adds providing a function table for the space adapted to exchange services with the library in the space, and further includes the step of employing the first and second threads to make function calls to the function table to access common data

between each of the planes and common data in the space. Claim 14 is not obvious from a hypothetical combination of Meyer, Cai and Arimilli for the reasons given in connection with claims 5, 11 and 12, discussed above.

It is respectfully submitted that the application has now been brought into a condition where allowance of the entire case is proper. Reconsideration and issuance of a notice of allowance are respectfully solicited.

Respectfully submitted,



Peter W. Peterson
Reg. No. 31,867

DeLIO & PETERSON, LLC
121 Whitney Avenue
New Haven, CT 06510-1241
(203) 787-0595

ibmf100273000amdA.doc